12-Bit Differential Input 200kSPS SAR ADC

ISL267817

The ISL267817 is a 12-bit, 200kSPS sampling SAR-type ADC which features excellent linearity over supply and temperature variations, and provides a drop-in compatible alternative to all ADS7817 performance grades. The robust, fully-differential input offers high impedance to minimize errors due to leakage currents, and the specified measurement accuracy is maintained with input signals up to the supply rails.

The reference accepts inputs between 0.1V to 2.5V, providing design flexibility in a wide variety of applications. The ISL267817 also features up to 8kV Human Body Model ESD survivability.

The serial digital interface is SPI compatible and is easily interfaced to all popular FPGAs and microcontrollers. Operating from a 5V supply, power dissipation is 2.15mW at a sampling rate of 200kSPS, and just 25µW between conversions utilizing the Auto Power-Down mode, making the ISL267817 an excellent solution for remote industrial sensors and battery-powered instruments. It is available in the compact, industry-standard 8 Lead SOIC package and is specified for operation over the industrial temperature range (-40°C to +85°C).

Features

- Drop-In Compatible with ADS7817 (All Performance Grades)
- Differential Input
- Simple SPI-compatible Serial Digital Interface
- Guaranteed No Missing Codes
- 200kHz Sampling Rate
- +4.75V to +5.25V Supply
- Low 2.15mW Operating Power (200kSPS)
- Power-down Current between Conversions: 3µA
- Excellent Differential Non-Linearity (1.0LSB max)
- Low THD: -85dB (typ)
- Pb-Free (RoHS Compliant)
- Available in SOIC Package

Applications

- Remote Data Acquisition
- Battery Operated Systems
- Industrial Process Control
- Energy Measurement
- Data Acquisition Systems
- Pressure Sensors
- Flow Controllers

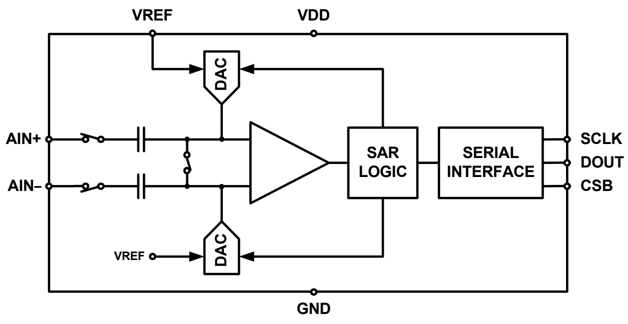


FIGURE 1. BLOCK DIAGRAM

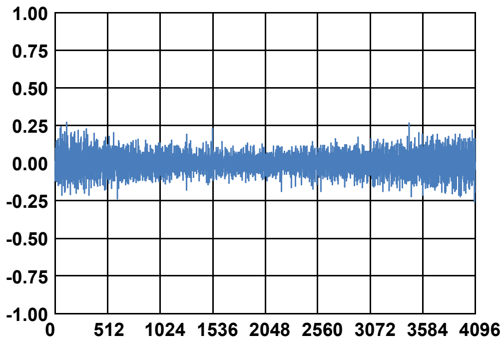
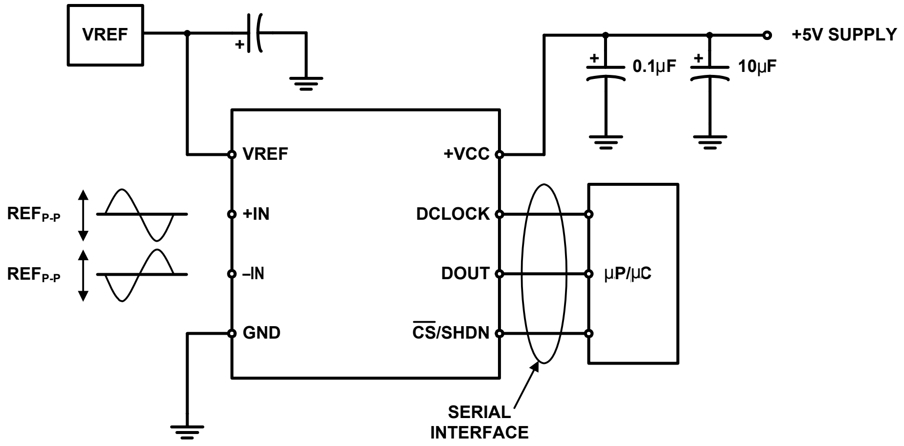


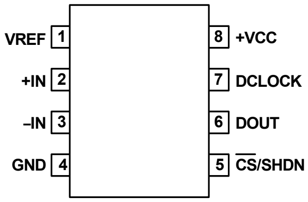
FIGURE 2. DIFFERENTIAL LINEARITY ERROR vs CODE

Typical Connection Diagram



Pin Configuration

ISL267817
(8 LD SOIC)
TOP VIEW



Pin Descriptions

PIN NAME	PIN NUMBER	DESCRIPTION
VREF	1	Reference Input
+IN	2	Non Inverting Input
–IN	3	Inverting Input
GND	4	Ground
$\overline{CS}$/SHDN	5	Low = Chip Select, High = Shutdown
DOUT	6	Serial Output Data
DCLOCK	7	Data Clock
+VCC	8	Power Supply

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	+VCC RANGE (V)	TEMP RANGE (°C)	PACKAGE	PKG. DWG. #
ISL267817IBZ	267817 IBZ	4.75 to 5.25	-40°C to +85°C	8 Ld SOIC	M8.15
Coming Soon ISL267817IUZ	67817	4.75 to 5.25	-40°C to +85°C	8 Ld MSOP	M8.118

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for the ISL267817. For more information on MSL please see tech brief TB363.

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Absolute Maximum Ratings

Any Pin to GND	-0.3V to +6.0V
Analog Input to GND	-0.3V to +VCC+0.3V
Digital I/O to GND	-0.3V to +VCC+0.3V
Digital Input Voltage to GND	-0.3V to +VCC+0.3V
Maximum Current In to Any Pin	10mA
ESD Rating	
Human Body Model (Tested per JESD22-A114F)	8kV
Machine Model (Tested per JESD22-A115B)	400V
Charged Device Model (Tested per JESD22-C101E)	1.5kV
Latch Up (Tested per JESD78C; Class 2, Level A)	100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld SOIC Package (Notes 4, 5)	120	64
8 Ld MSOP Package (Notes 4, 5)	165	64

Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Junction Temperature	+150°C
Pb-Free Reflow Profile	see link below

http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications

+VCC = +5V, f_{DCLOCK} = 3.2MHz, f_S = 200kSPS, V_{REF} = 2.5V; V_{CM} = V_{REF}, Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
ANALOG INPUT (Note 7)						
|AIN|	Full-Scale Input Span	+IN – (–IN)	**-VREF**		**+VREF**	V
	Absolute Input Voltage	+IN	**-0.3**		**+VCC +0.3**	V
		–IN	**-0.3**		**+VCC +0.3**	V
C_{VIN}	Input Capacitance	Sample/Hold Mode		13/6		pF
I_{LEAK}	Input DC Leakage Current		**-1**	0.01	**1**	µA
SYSTEM PERFORMANCE						
N	Resolution		**12**			Bits
	No Missing Codes		**12**			Bits
INL	Integral Nonlinearity		**-1**	±0.5	**1**	LSB
DNL	Differential Nonlinearity		**-1**	±0.4	**1**	LSB
OFFSET	Zero-Code Error		**-6**	±0.25	**6**	LSB
GAIN	Gain Error		**-4**	±0.12	**4**	LSB
CMRR	Common-Mode Rejection			80		dB
PSRR	Power Supply Rejection			82		dB
SAMPLING DYNAMICS						
t_{CONV}	Conversion Time	f_{DCLOCK} = 3.2MHz			**12**	Clk Cycles
t_{ACQ}	Acquisition Time		**1.5**			Clk Cycles
f_{max}	Throughput Rate				**200**	kSPS
DYNAMIC CHARACTERISTICS						
THD	Total Harmonic Distortion	V_{IN} = 5.0Vpp at f_{IN} = 1kHz		-85		dB
		V_{IN} = 5.0Vpp at f_{IN} = 5kHz		-84		dB
SINAD	Signal-to (Noise + Distortion) Ratio	V_{IN} = 5.0Vpp at f_{IN} = 1kHz		71		dB
SFDR	Spurious Free Dynamic Range	V_{IN} = 5.0Vpp at f_{IN} = 1kHz		85		dB
BW	Full Power Bandwidth	@ –3dB		15		MHz

Electrical Specifications

+VCC = +5V, f_{DCLOCK} = 3.2MHz, f_S = 200kSPS, V_{REF} = 2.5V; V_{CM} = V_{REF}, Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
REFERENCE INPUT						
REF	REF Input Range		**0.1**		**2.5**	V
REFLEAK	Current Drain		**-100**	4	**100**	µA
		f_{SAMPLE} = 12.5kHz	**-20**	0.23	**20**	µA
		$\overline{CS}$/SHDN = +VCC	**-3**	0.01	**3**	µA
DIGITAL INPUT/OUTPUT						
	Logic Family		CMOS			
V_{IH}	Input High Voltage		**3**		**+VCC + 0.3**	V
V_{IL}	Input Low Voltage		**-0.3**		**0.8**	V
V_{OH}	Output High Voltage	I_{OH} = −250µA	**3.5**			V
V_{OL}	Output Low Voltage	I_{OL} = 250µA			**0.4**	V
	Output Coding		Two's Complement			
I_{LEAK}	Input Leakage Current		**-1**		**1**	µA
C_{IN}	Input Capacitance			10		pF
I_{OZ}	Floating-State Output Current		**-1**		**1**	µA
C_{OUT}	Floating-State Output Capacitance			5		pF
POWER REQUIREMENTS						
V_{CC}	Supply Voltage Range		**4.75**		**5.25**	V
I_{CC}	Supply Current			430	**800**	µA
		f_{SAMPLE} = 12.5kHz (Notes 8, 9)		38		µA
		f_{SAMPLE} = 12.5kHz (Note 9)		223		µA
	Power Down Current	$\overline{CS}$/SHDN = +VCC, f_{SAMPLE} = 0Hz		0.5	**3**	µA
TEMPERATURE RANGE						
	Specified Performance		**-40**		**+85**	°C

NOTES:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
7. The absolute voltage applied to each analog input must be between GND and +VCC to guarantee datasheet performance.
8. f_{DCLOCK} = 3.2MHz, $\overline{CS}$/SHDN = +VCC for 241 clock cycles out of every 256.
9. See "Power vs Throughput Rate" on page 13 for more information regarding lower sample rates.

Timing Specifications

Limits established by characterization and are not production tested. +VCC = 5V, f_{DCLOCK} = 3.2MHz, f_S = 200kSPS, V_{REF} = 2.5V; V_{CM} = V_{REF}. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
t_{SMPL}	Analog Input Sample Time		**1.5**		**2.0**	Clk Cycles
t_{CONV}	Conversion Time			12		Clk Cycles
f_{CYC}	Throughput Rate				**200**	kHz
t_{CSD}	$\overline{CS}$/SHDN Falling Edge to DCLOCK Low				**0**	ns
t_{SUCS}	$\overline{CS}$/SHDN Falling Edge to DCLOCK Rising Edge		**30**			ns
t_{hDO}	DCLOCK Falling Edge to Current DOUT Not Valid		**15**			ns

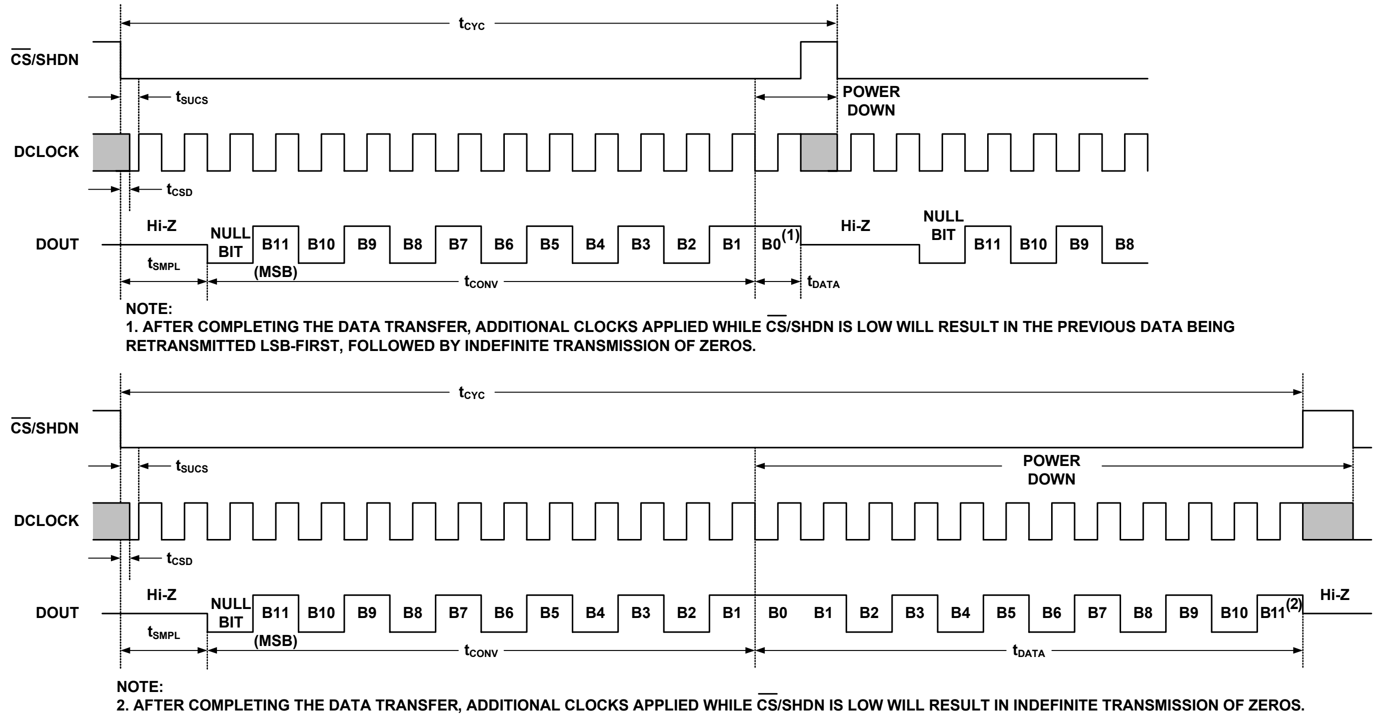
Timing Specifications

Limits established by characterization and are not production tested. +VCC = 5V, f_{DCLOCK} = 3.2MHz, f_S = 200kSPS, V_{REF} = 2.5V; V_{CM} = V_{REF}. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
t_{dDO}	DCLOCK Falling Edge to Next DOUT Valid			35	**150**	ns
t_{DIS}	$\overline{CS}$/SHDN Rising Edge to DOUT Disable Time	See Note 10		40	**50**	ns
t_{EN}	DCLOCK Falling Edge to DOUT Enabled			22	**100**	ns
t_f	DCLOCK Fall Time			1	**100**	ns
t_r	DCLOCK Rise Time			1	**100**	ns

NOTE:

10. During characterization, t_{DIS} is measured from the release point with a 10pF load (see Figure 4) and the equivalent timing using the ADS7817 loading (3kΩ, 100pF) is calculated.



NOTE:

1. AFTER COMPLETING THE DATA TRANSFER, ADDITIONAL CLOCKS APPLIED WHILE $\overline{CS}$/SHDN IS LOW WILL RESULT IN THE PREVIOUS DATA BEING RETRANSMITTED LSB-FIRST, FOLLOWED BY INDEFINITE TRANSMISSION OF ZEROS.

NOTE:

2. AFTER COMPLETING THE DATA TRANSFER, ADDITIONAL CLOCKS APPLIED WHILE $\overline{CS}$/SHDN IS LOW WILL RESULT IN INDEFINITE TRANSMISSION OF ZEROS.

FIGURE 3. SERIAL INTERFACE TIMING DIAGRAM

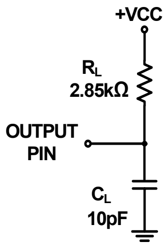


FIGURE 4. EQUIVALENT LOAD CIRCUIT

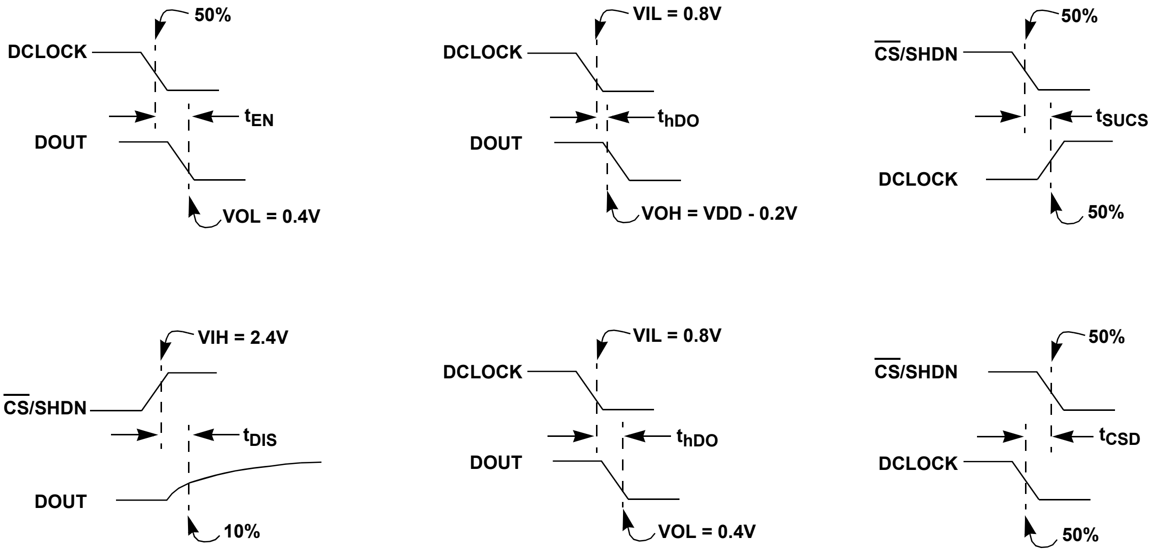


FIGURE 5. TIMING PARAMETER DEFINITIONS

Typical Performance Characteristics

$T_A = +25°C$, $V_{CC} = 5V$, $V_{REF} = 2.5V$, $f_{SAMPLE} = 200kHz$, $f_{CLK} = 16 * f_{SAMPLE}$, unless otherwise specified.

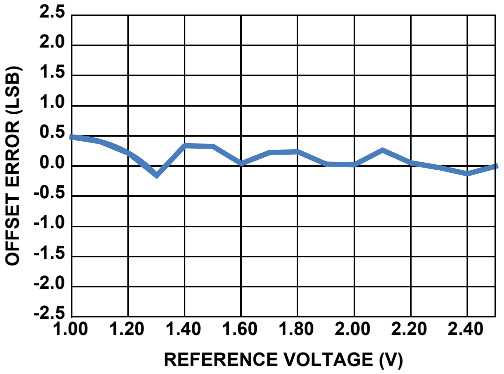


FIGURE 6. CHANGE IN OFFSET vs REFERENCE VOLTAGE

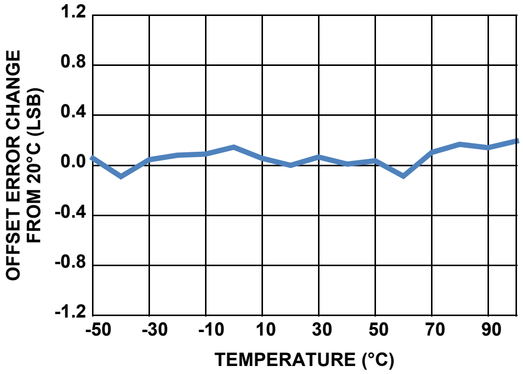


FIGURE 7. CHANGE IN OFFSET vs TEMPERATURE

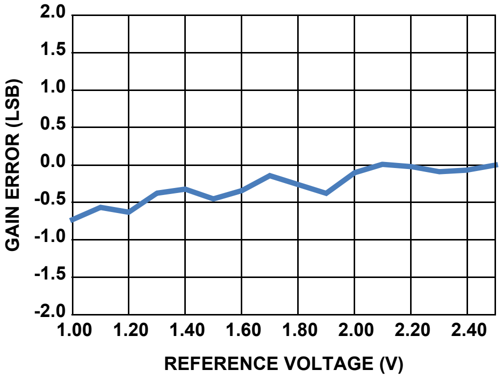


FIGURE 8. CHANGE IN GAIN vs REFERENCE VOLTAGE

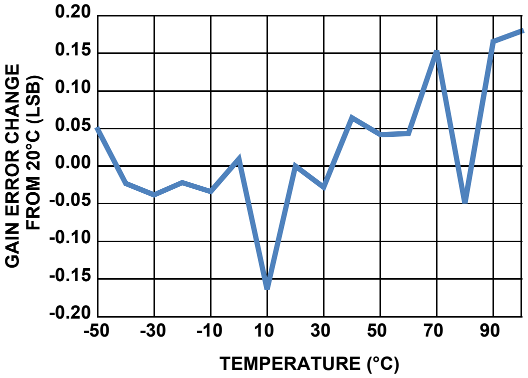


FIGURE 9. CHANGE IN GAIN vs TEMPERATURE

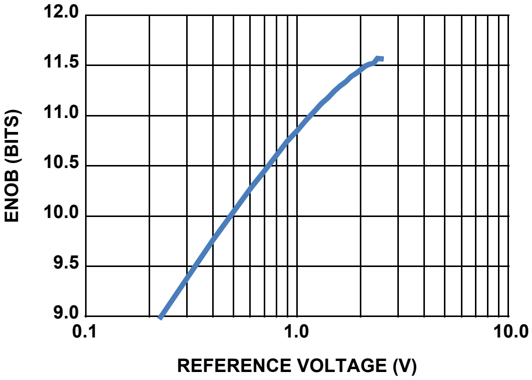


FIGURE 10. EFFECTIVE NUMBER OF BITS vs REFERENCE VOLTAGE

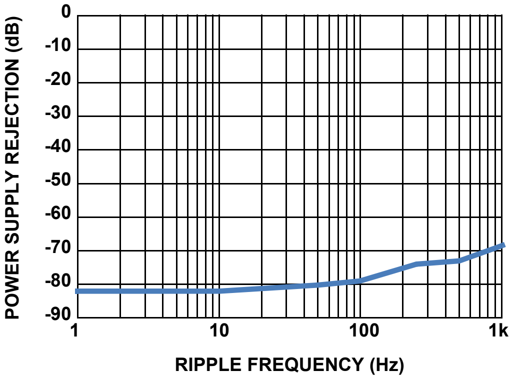


FIGURE 11. POWER SUPPLY REJECTION vs RIPPLE FREQUENCY

Typical Performance Characteristics

$T_A = +25°C$, $V_{CC} = 5V$, $V_{REF} = 2.5V$, $f_{SAMPLE} = 200kHz$, $f_{CLK} = 16 * f_{SAMPLE}$, unless otherwise specified. **(Continued)**

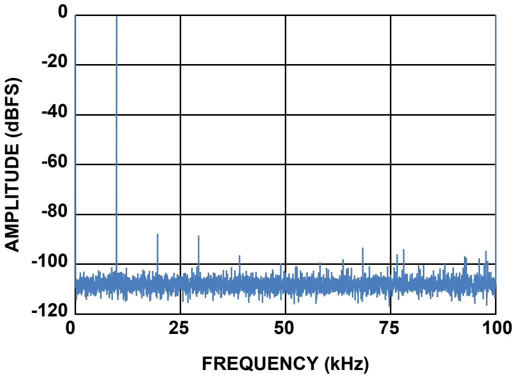


FIGURE 12. FREQUENCY SPECTRUM (8192 POINT FFT; f_{IN} = 9.9kHz, −0.5dB

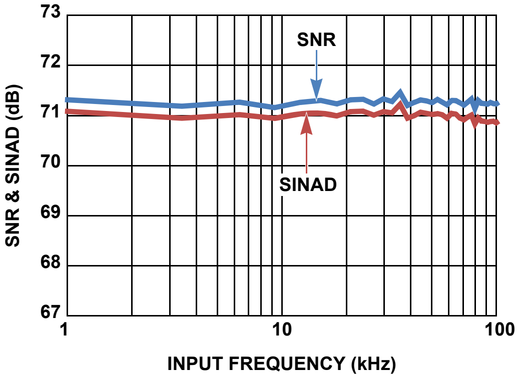


FIGURE 13. SIGNAL-TO-NOISE RATIO AND SIGNAL-TO-(NOISE+DISTORTION) vs INPUT FREQUENCY

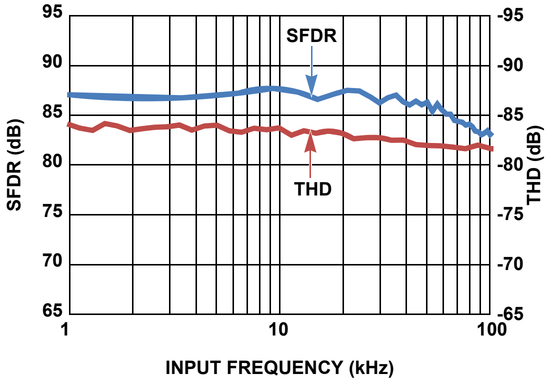


FIGURE 14. SPURIOUS FREE DYNAMIC RANGE AND TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY

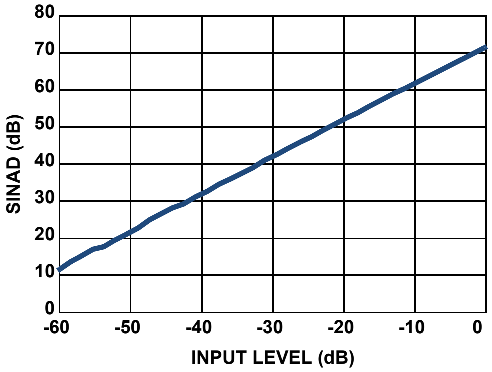


FIGURE 15. SIGNAL-TO-(NOISE+DISTORTION) vs INPUT LEVEL

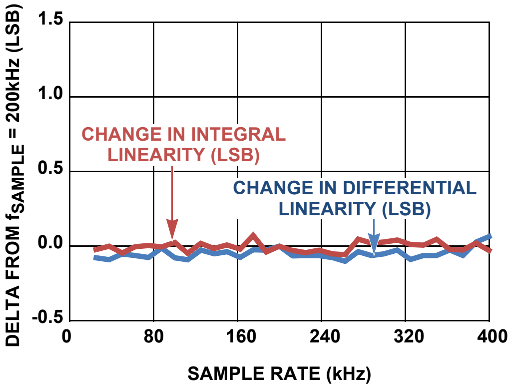


FIGURE 16. CHANGE IN INTEGRAL LINEARITY and DIFFERENTIAL LINEARITY vs SAMPLE RATE

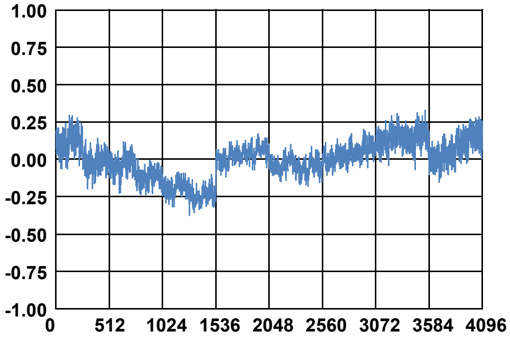


FIGURE 17. INTEGRAL LINEARITY ERROR vs CODE

Typical Performance Characteristics

$T_A = +25°C$, $V_{CC} = 5V$, $V_{REF} = 2.5V$, $f_{SAMPLE} = 200kHz$, $f_{CLK} = 16 * f_{SAMPLE}$, unless otherwise specified. **(Continued)**

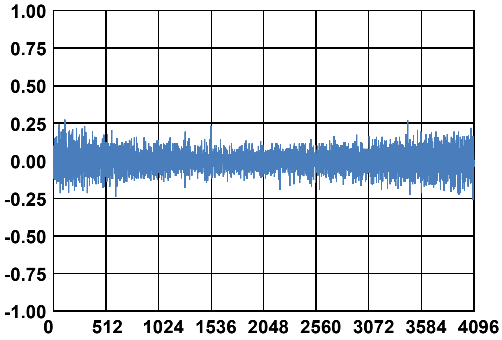


FIGURE 18. DIFFERENTIAL LINEARITY ERROR vs CODE

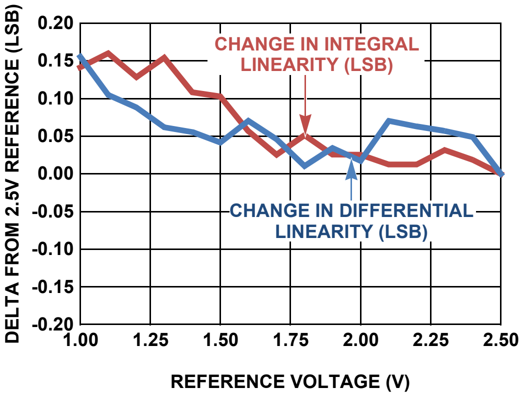


FIGURE 19. CHANGE IN INTEGRAL LINEARITY AND DIFFERENTIAL LINEARITY vs REFERENCE VOLTAGE

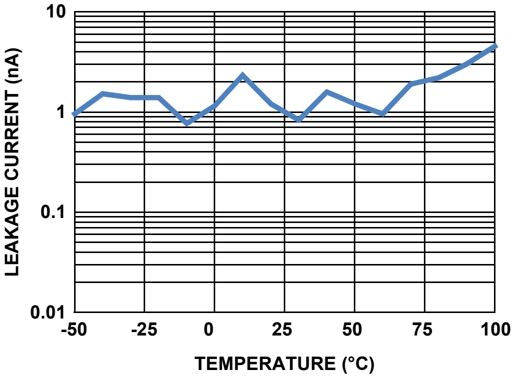


FIGURE 20. INPUT LEAKAGE CURRENT vs TEMPERATURE

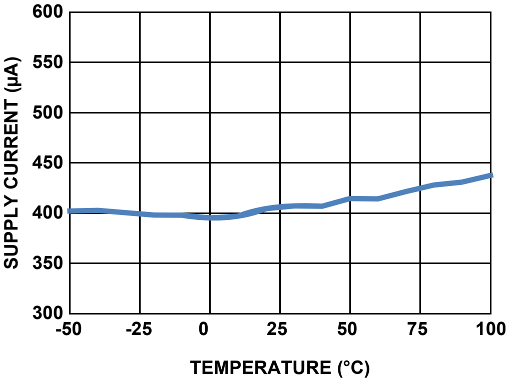


FIGURE 21. SUPPLY CURRENT vs TEMPERATURE

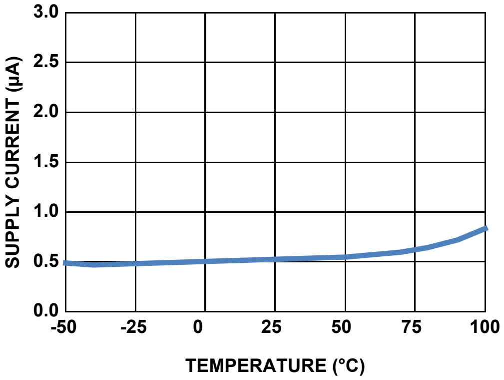


FIGURE 22. POWER DOWN SUPPLY CURRENT vs TEMPERATURE

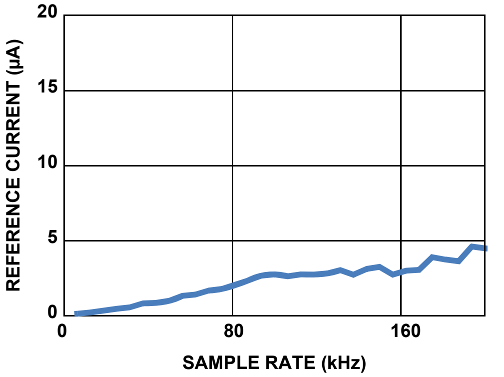


FIGURE 23. REFERENCE CURRENT vs SAMPLE RATE (CODE = FF8h)

Typical Performance Characteristics

T_A = +25°C, V_{CC} = 5V, V_{REF} = 2.5V, f_{SAMPLE} = 200kHz, f_{CLK} = 16 * f_{SAMPLE}, unless otherwise specified. **(Continued)**

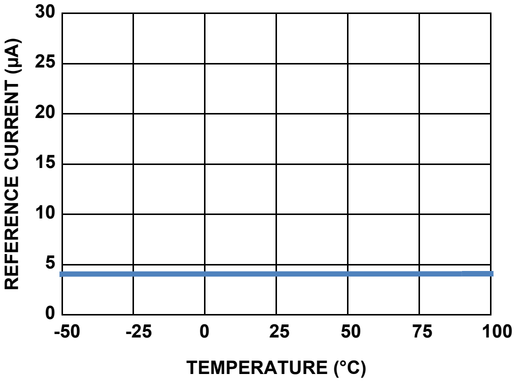


FIGURE 24. REFERENCE CURRENT vs TEMPERATURE (CODE = FF8h)

Functional Description

The ISL267817 is based on a successive approximation register (SAR) architecture utilizing capacitive charge redistribution digital to analog converters (DACs). Figure 25 shows a simplified representation of the converter. During the acquisition phase (ACQ), the differential input is stored on the sampling capacitors (CS). The comparator is in a balanced state since the switch across its inputs is closed. The signal is fully acquired after t_{ACQ} has elapsed, and the switches then transition to the conversion phase (CONV) so the stored voltage may be converted to digital format. The comparator will become unbalanced when the differential switch opens and the input switches transition (assuming that the stored voltage is not exactly at mid-scale). The comparator output reflects whether the stored voltage is above or below mid-scale, which sets the value of the MSB. The SAR logic then forces the capacitive DACs to adjust up or down by one quarter of full-scale by switching in binarily weighted capacitors. Again, the comparator output reflects whether the stored voltage is above or below the new value, setting the value of the next lowest bit. This process repeats until all 12 bits have been resolved.

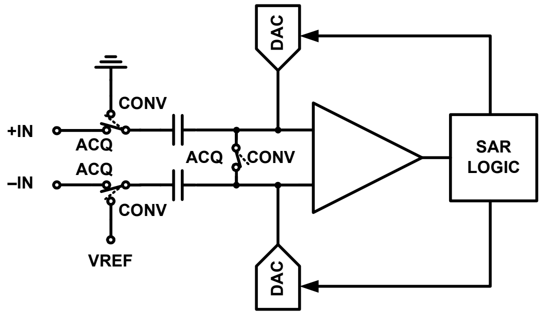


FIGURE 25. SAR ADC ARCHITECTURAL BLOCK DIAGRAM

An external clock must be applied to the DCLOCK pin to generate a conversion result. The allowable frequency range for DCLOCK is 10kHz to 3.2MHz (625SPS to 200kSPS). Serial output data is transmitted on the falling edge of DCLOCK. The receiving device (FPGA, DSP or Microcontroller) may latch the data on the rising edge of DCLOCK to maximize set-up and hold times.

A stable, low-noise reference voltage must be applied to the VREF pin to set the full-scale input range and common-mode voltage. See “Voltage Reference Input” on page 12 for more details.

ADC Transfer Function

The output coding for the ISL267817 is twos complement. The first code transition occurs at successive LSB values (i.e., 1 LSB, 2 LSB, and so on). The LSB size is 2*VREF/4096. The ideal transfer characteristic of the ISL267817 is shown in Figure 26.

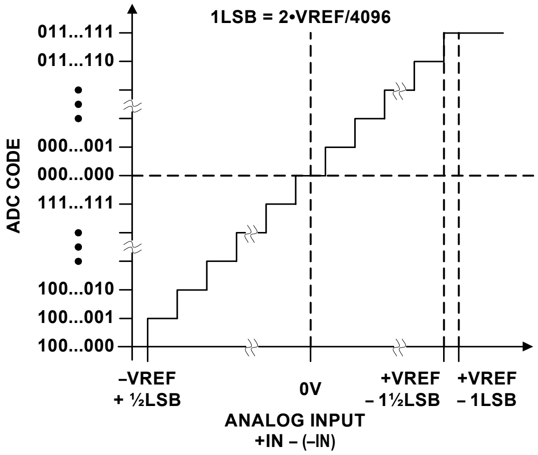


FIGURE 26. IDEAL TRANSFER CHARACTERISTICS

Analog Input

The ISL267817 features a fully differential input with a nominal full-scale range equal to twice the applied VREF voltage. Each input swings VREF Vpp, 180° out-of-phase from one another for a total differential input of 2*VREF (refer to Figure 27).

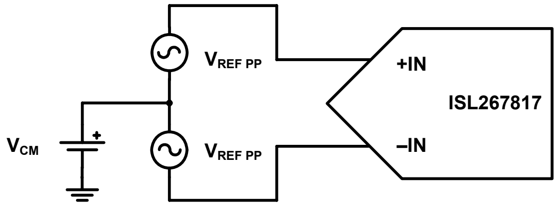


FIGURE 27. DIFFERENTIAL INPUT SIGNALING

Differential signaling offers several benefits over a single-ended input, such as:

- Doubling of the full-scale input range (and therefore the dynamic range)
- Improved even order harmonic distortion
- Better noise immunity due to common mode rejection

Figure 28 shows the relationship between the reference voltage and the full-scale input range for two different values of VREF. Note that there is a trade-off between VREF and the allowable common mode input voltage (VCM). The full-scale input range is proportional to VREF; therefore the VCM range must be limited for larger values of VREF in order to keep the absolute maximum and minimum voltages on the +IN and –IN pins within specification. Figures 29 and 30 illustrate this relationship for single-ended and differential inputs, respectively.

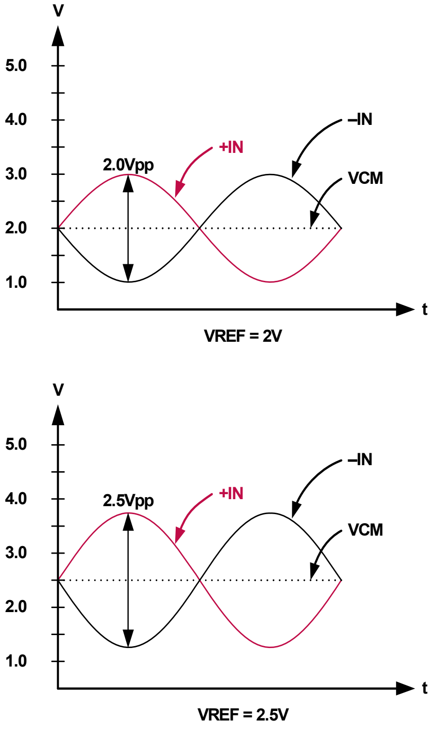


FIGURE 28. RELATIONSHIP BETWEEN VREF AND FULL-SCALE RANGE

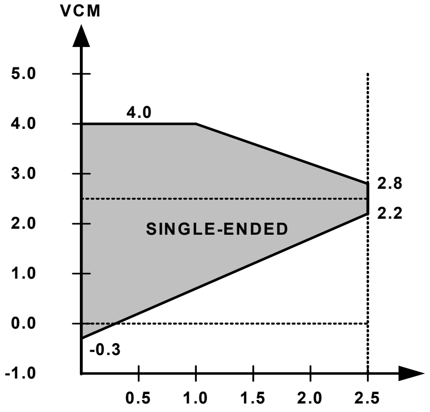


FIGURE 29. RELATIONSHIP BETWEEN VREF AND VCM FOR SINGLE-ENDED INPUTS (+VCC = 5V)

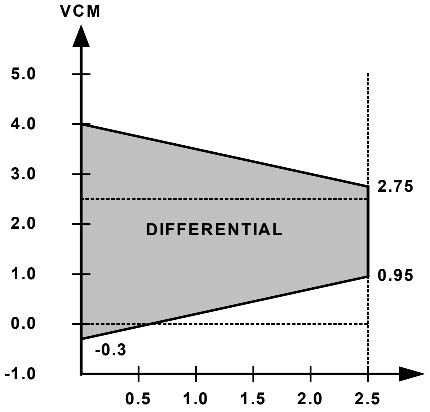


FIGURE 30. RELATIONSHIP BETWEEN VREF AND VCM FOR DIFFERENTIAL INPUTS (+VCC = 5V)

Voltage Reference Input

An external low-noise reference voltage must be applied to the VREF pin to set the full-scale input range of the converter. The reference input accepts voltages ranging from 0.1V to 2.5V; however the device is specified with a reference voltage of 2.5V. This pin should be decoupled with a combination of a 1µF electrolytic capacitor and a 0.1µF ceramic capacitor on the PC board.

Since the full-scale input range is proportional to the applied VREF, any noise or drift will appear as an error in the conversion result. A low-noise, low-drift reference such as the ISL2100x family may be used to maximize system performance, as shown in Figure 31. The VREF pin typically draws 4µA and the current is dependent upon the sampled voltage. This can result in a code-dependent error if there is excessive series resistance or the reference lacks sufficient load regulation; therefore, buffering may be necessary.

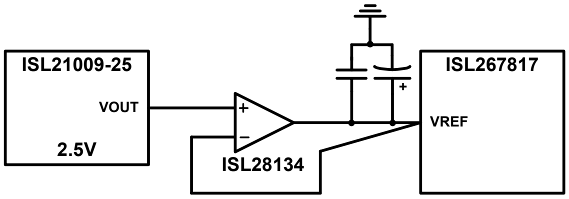


FIGURE 31. BUFFERED VOLTAGE REFERENCE

Power-Down/Standby Modes

The mode of operation of the ISL267817 is selected by controlling the logic state of the $\overline{\text{CS}}$/SHDN signal during a conversion. There are two possible modes of operation: dynamic mode or static mode. When $\overline{\text{CS}}$/SHDN is high (deasserted), the ADC will be in static mode. Conversely, when $\overline{\text{CS}}$/SHDN is low (asserted), the device will be in dynamic mode. There are no minimum or maximum number of DCLOCK cycles required to enter static mode, which simplifies power management and allows the user to easily optimize power dissipation versus throughput for different application requirements.

DYNAMIC MODE

This mode is entered when a conversion result is desired by asserting $\overline{\text{CS}}$/SHDN. Figure 32 shows the general diagram of operation in this mode. The conversion is initiated on the falling edge of $\overline{\text{CS}}$/SHDN, as described in the “Serial Digital Interface” section on page 14. As soon as $\overline{\text{CS}}$/SHDN is brought high, the conversion will be terminated and DOUT will go back into three-state. Sixteen serial clock cycles are required to complete the conversion and access the complete conversion result. $\overline{\text{CS}}$/SHDN may idle high until the next conversion or idle low until sometime prior to the next conversion. Once a data transfer is complete, i.e., when DOUT has returned to three-state, another conversion can be initiated by again bringing $\overline{\text{CS}}$/SHDN low.

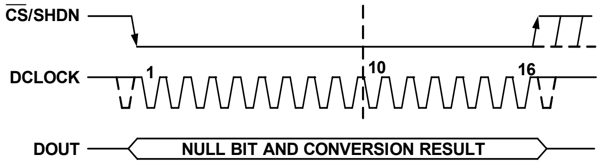


FIGURE 32. NORMAL MODE OPERATION

STATIC MODE

The ISL267817 enters the power-saving static mode automatically any time $\overline{\text{CS}}$/SHDN is deasserted. It is not required that the user force a device into this mode following a conversion in order to optimize power consumption.

SHORT CYCLING

In cases where a lower resolution conversion is acceptable, $\overline{\text{CS}}$/SHDN can be pulled high before 12 DCLOCK falling edges have elapsed. This is referred to as short cycling, and it can be used to further optimize power dissipation. In this mode, a lower resolution result will be acquired, but the ADC will enter static mode sooner and exhibit a lower average power dissipation than if the complete conversion cycle were carried out. The acquisition time (t_{ACQ}) requirement must be met for the next conversion to be valid.

POWER-ON RESET

The ISL267817 performs a power-on reset when the supplies are first activated, which requires approximately 2.5ms to execute. After this is complete, a single dummy cycle must be executed in order to initialize the switched capacitor track and hold. A dummy cycle will take 5µs with an 3.2MHz DCLOCK. Once the dummy cycle is complete, the ADC mode will be determined by the state of $\overline{\text{CS}}$/SHDN. At this point, switching between dynamic and static modes is controlled by $\overline{\text{CS}}$/SHDN with no delay required between states.

POWER vs THROUGHPUT RATE

The ISL267817 provides reduced power consumption at lower conversion rates by automatically switching into a low-power mode after completing a conversion. Maximum power savings are achieved by running SCLK at the maximum rate, as shown in Figure 33. If SCLK is operated at a fixed 16x multiple of the sample rate then the average power consumption of the ADC is roughly constant, decreasing somewhat at lower throughput rates (Figure 34).

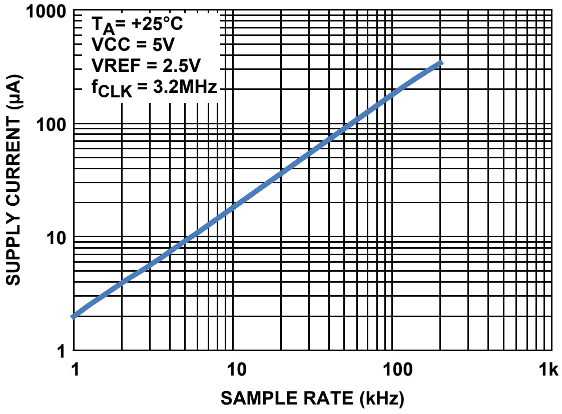


FIGURE 33. POWER CONSUMPTION vs SAMPLE RATE, f_{CLK} = 3.2MHZ

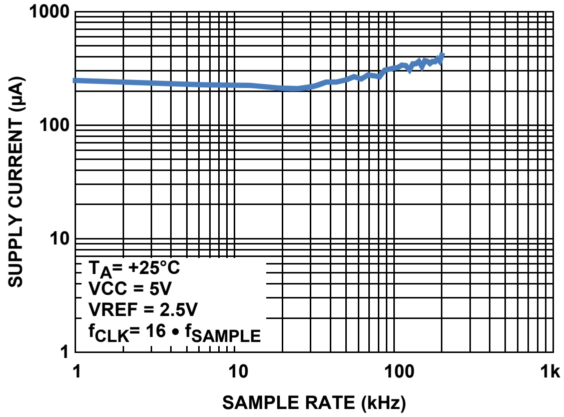


FIGURE 34. SHUTDOWN CURRENT vs SAMPLE RATE, f_{CLK} = 16 • f_{SAMPLE}

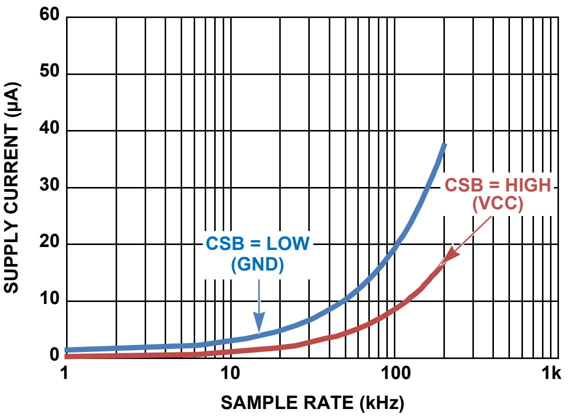


FIGURE 35. SHUTDOWN CURRENT vs SAMPLE RATE

The shutdown current is impacted by the state of the $\overline{\text{CS}}$/SHDN pin, as shown in Figure 35.

Serial Digital Interface

Conversion data is accessed with an SPI-compatible serial interface. The interface consists of the data clock (DCLOCK), serial data output (DOUT), and chip select/shutdown ($\overline{\text{CS}}$/SHDN).

A falling edge on the $\overline{\text{CS}}$/SHDN signal initiates a conversion by placing the part into the acquisition (ACQ) phase. After t_{ACQ} has elapsed, the part enters the conversion (CONV) phase and begins outputting the conversion result starting with a null bit followed by the most significant bit (MSB) and ending with the least significant bit (LSB). The $\overline{\text{CS}}$/SHDN pin can be pulled high at this point to put the device into Standby mode and reduce the power consumption. If $\overline{\text{CS}}$/SHDN is held low after the LSB bit has been output, the conversion result will be repeated in reverse order until the MSB is transmitted, after which the serial output enters a high impedance state. The ISL267817 will remain in this state, dissipating typical dynamic power levels, until $\overline{\text{CS}}$/SHDN transitions high then low to initiate the next conversion.

Data Format

Output data is encoded in two's complement format, as shown in Table 1. The voltage levels in the table are idealized and don't account for any gain/offset errors or noise.

TABLE 1. TWO'S COMPLEMENT DATA FORMATTING

INPUT	VOLTAGE	DIGITAL OUTPUT
-Full Scale	-VREF	1000 0000 0000
-Full Scale + 1LSB	-VREF+ ½ LSB	1000 0000 0001
Midscale	0	0000 0000 0000
+Full Scale - 1LSB	+VREF- 1½ LSB	0111 1111 1110
+Full Scale	+VREF - ½ LSB	0111 1111 1111

Applications Information

Adjustable Low-Noise Reference

Figure 36 illustrates how a Digitally Controlled Potentiometer (DCP) can be used in conjunction with a low-noise, low-drift reference to realize an adjustable input range with high system accuracy. The voltage reference output is connected to the high terminal of the DCP and the wiper terminal is buffered and connected to the ADC reference. Buffering is required since the ISL267817 reference input current will cause a voltage drop across the DCP element (100kΩ from RH to RL), impacting accuracy and increasing temperature drift.

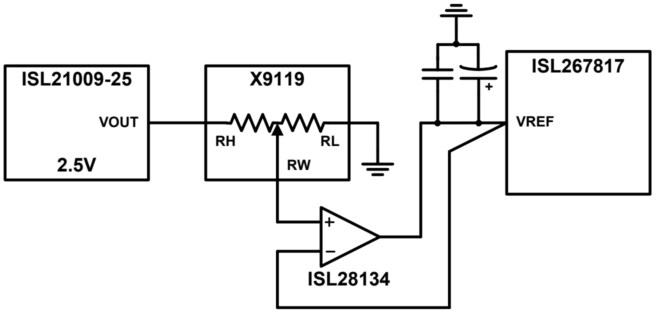


FIGURE 36. ADJUSTABLE BUFFERED VOLTAGE REFERENCE

TERMINOLOGY

Signal-to-(Noise + Distortion) Ratio (SINAD)

This is the measured ratio of signal-to-(noise + distortion) at the output of the ADC. The signal is the RMS amplitude of the fundamental. Noise is the sum of all non-fundamental signals up to half the sampling frequency ($f_S/2$), excluding DC. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by Equation 1:

$$\text{Signal-to-(Noise + Distortion)} = (6.02\ N + 1.76)\text{dB} \qquad \text{(EQ. 1)}$$

Thus, for a 12-bit converter this is 74dB, and for a 10-bit this is 62dB.

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of harmonics to the fundamental. For the ISL267817, it is defined as:

$$\text{THD(dB)} = 20\log\sqrt{\frac{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}{V_1^2}} \qquad \text{(EQ. 2)}$$

where V_1 is the RMS amplitude of the fundamental and V_2, V_3, V_4, V_5, and V_6 are the RMS amplitudes of the second to the sixth harmonics.

Peak Harmonic or Spurious Noise (SFDR)

Peak harmonic or spurious noise is defined as the ratio of the RMS value of the next largest component in the ADC output spectrum (up to fs/2 and excluding DC) to the RMS value of the fundamental. Also referred to as Spurious Free Dynamic Range (SFDR). Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

Full Power Bandwidth

The full power bandwidth of an ADC is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full-scale input.

Common-Mode Rejection Ratio (CMRR)

The common-mode rejection ratio is defined as the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 250mV$_{P-P}$ sine wave applied to the common-mode voltage of +IN and −IN of frequency fs:

$$CMRR(dB) = 10\log(Pfl/Pfs) \qquad \text{(EQ. 3)}$$

Pf is the power at the frequency f in the ADC output; *Pfs* is the power at frequency fs in the ADC output.

Integral Nonlinearity (INL)

This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity (DNL)

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Zero-Code Error

This is the deviation of the midscale code transition (111...111 to 000...000) from the ideal +IN – (–IN) (i.e., 0 LSB).

Gain Error

This is the deviation of the first code transition (100...000 to 100...001) from the ideal +IN – (–IN) (i.e., – VREF + ½ LSB) or the last code transition (011...110 to 011...111) from the ideal +IN – (–IN) (i.e., +VREF – 1½ LSB), after the zero code error has been adjusted out.

Track and Hold Acquisition Time

The track and hold acquisition time is the minimum time required for the track and hold amplifier to remain in track mode for its output to reach and settle to within 0.5 LSB of the applied input signal.

Power Supply Rejection Ratio (PSRR)

The power supply rejection ratio is defined as the ratio of the power in the ADC output at full-scale frequency, f, to ADC +VCC supply of frequency f_S. The frequency of this input varies from 1kHz to 1MHz.

$$PSRR(dB) = 10\log(Pf/Pfs) \qquad \text{(EQ. 4)}$$

Pf is the power at frequency f in the ADC output; *Pfs* is the power at frequency f_S in the ADC output.

Application Hints

Grounding and Layout

The printed circuit board that houses the ISL267817 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. A minimum etch technique is generally best for ground planes since it gives the best shielding. Digital and analog ground planes should be joined in only one place, and the connection should be a star ground point established as close to the GND pin on the ISL267817 as possible. Avoid running digital lines under the device, as this will couple noise onto the die. The analog ground plane should be allowed to run under the ISL267817 to avoid noise coupling.

The power supply lines to the device should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line.

Fast switching signals, such as clocks, should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best but is not always possible with a double-sided board.

In this technique, the component side of the board is dedicated to ground planes, while signals are placed on the solder side.

Good decoupling is also important. All analog supplies should be decoupled with 10µF tantalum capacitors in parallel with 0.1µF capacitors to GND. To achieve the best from these decoupling components, they must be placed as close as possible to the device.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
October 28, 2011	FN7877.0	Initial Release

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL267817

To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

FITs are available from our website at: http://rel.intersil.com/reports/search.php

For additional products, see www.intersil.com/product_tree

Intersil products are manufactured, assembled and tested utilizing ISO9000 quality systems as noted
in the quality certifications found at www.intersil.com/design/quality

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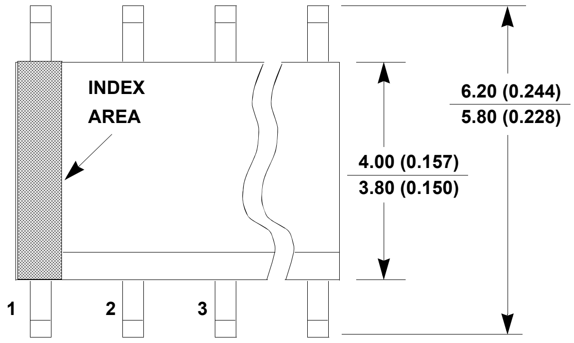
Package Outline Drawing

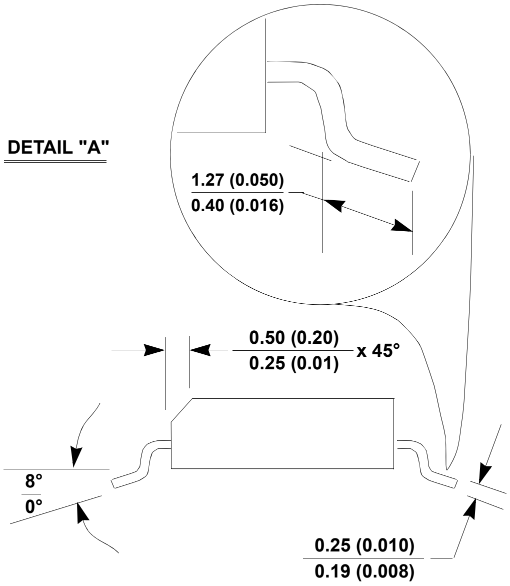
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

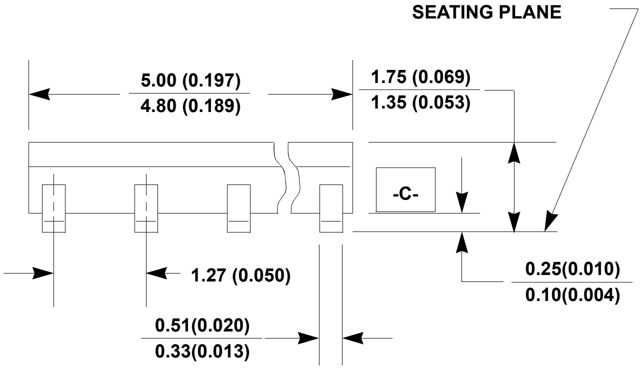
Rev 3, 3/11



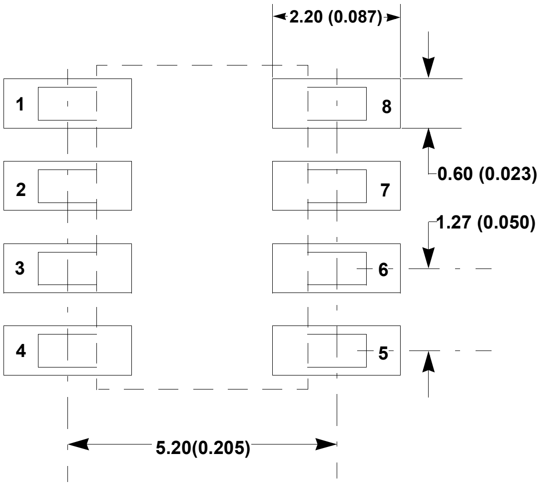
TOP VIEW



SIDE VIEW “B”



SIDE VIEW “A



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.